Supplementary Information

High performance electronics using dense, perfectly aligned arrays of single walled carbon nanotubes
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Growth of SWNT arrays and fabrication of array devices
The procedures outlined in the main text lead to SWNT arrays that have extremely high levels of perfection, as determined by the degree of alignment and the degree of linearity in the shapes of the SWNTs, even at values of $D$ that approach 10 SWNT/µm. Figure S1 provides various measurements of a typical SWNT array that quantify the degree of alignment, the degree of linearity, the diameter distribution, the length distribution and the approximate ratio of metallic to semiconducting tubes. Figure S1i presents some statistical information on the extent of variation in the properties of devices formed with these arrays, using electrode geometries and fabrication procedures outlined in the part of the main text that describes Fig. 1. We performed extensive SEM analysis to examine the yields and extent of variation in the SWNT arrays grown using similar procedures on multiple substrates. Figure S2 provides representative results, illustrating the high level of reproducibility in the growth procedures. (The ‘wavy’ shapes of the catalyst lines apparent in the low magnification views result from charging during the collection of the SEM images.)

Fabrication of single tube devices
To provide further data to compare to our array devices, we fabricated single tube devices using aligned arrays of SWNT grown on quartz and then transferred to SiO$_2$(100 nm)/Si. Photolithography defined Ti (1 nm)/Pd (20 nm) source and drain electrodes onto these arrays. We then protected individual SWNTs in the array with 2 µm wide stripes of photoresist (AZ 5214) and then etched away all of the unprotected SWNTs with oxygen reactive ion etching (RIE). The photoresist was then removed with acetone and isopropyl alcohol. We collected SEM images to verify that there is only one SWNT bridging the S/D electrodes. Figure S3 provides an SEM image and measured transfer curves. The devices operate in p channel mode, consistent with observations in array devices. Also, the calculated mobility is in the same range as the average tube mobility inferred from array devices.
Measurements of dielectric constants

Metal-insulator-metal structures were used to measure the dielectric constant of the polyimide (PI) gate dielectric. We used Au top and bottom contacts defined by photolithography and lift-off. The PI was spin cast at 5000 rpm for 30 s and cured at 150 °C for 5 hours. The thickness of the PI layer was measured by surface profilometry (Sloan Dektak3 ST). To open the bottom electrode for probing, RIE etching was used to remove locally the PI. The capacitance of the resulting structure was measured using an Agilent 4288A Capacitance Meter. By using the equation $C = \frac{\varepsilon \varepsilon_0}{d}$, dielectric constant was obtained (3.2). For the BCB/HfO$_2$ bilayer dielectrics, we fabricated the same electrode structure to measure the capacitance. The thicknesses of the BCB (~20nm) and HfO$_2$ (~10 nm) layers were measured by AFM (DI, Dimension 3100). The dielectric constant for the BCB inferred from these measurements is somewhat higher than values reported in the literature, due possibly to modifications induced in the BCB during the atomic layer deposition of the HfO$_2$.

On/off ratio vs. channel length

Even though more than 99.9% of the m- and s-SWNTs are aligned, to within < 0.01 degree, the on/off ratio of these devices is observed to be systematically increasing with channel length ($L$), as shown in Fig. S4. This is unexpected because the ratio of the number of m- and s-SWNTs (~1/3) is independent of channel length.

Below we show that the presence of significant contact resistance plays an important role in determining the on/off ratio. The resistance of an individual m-SWNT can be written as $R_M + \rho_M L$ and the resistance of an individual s-SWNT can be written as $R_S + \rho_S L$, where, $R_M$ and $R_S$ are m- and s-SWNT contact resistance per tube, respectively, while $\rho_M$ and $\rho_S$ are m- and s-SWNT resistance per unit length of the tube. Hence the total current through all the m-SWNTs can be written as

$$I_m = f_M N V_D / (R_M + \rho_M L)$$

where, $f_M$ is fraction of m-SWNTs and $N$ is total number of tubes in a device. A similar equation can be written for s-SWNT as well.

The on/off Ratio $(S)$ can be written as
\[ S = \frac{I_{\text{on}}}{I_{\text{off}}} = 1 + \frac{I_s + I_m}{I_m} = 1 + \frac{f_s/NV_D}{f_M/NV_D} \frac{(R_S + \rho_s L)}{(R_M + \rho_M L)} \]  
Eq. (2)

Eq. (2) can be rearranged as,

\[ S = 1 + \left( \frac{R_M + \rho_M L}{R_s + \rho_s L} \right) \frac{f_s}{f_M} \]  

Note that Eq. (3) can be independent of \( L \) only if \( R_M = R_S = 0 \) or \( R_M/R_S = \rho_M/\rho_S \). Both of these conditions may not be true for every given device. Considering the limiting cases,

\[ S(L \to 0) = 1 + \left( \frac{R_M}{R_s} \right) \frac{f_s}{f_M} \]  

\[ S(L \to \infty) = 1 + \left( \frac{\rho_M}{\rho_s} \right) \frac{f_s}{f_M} \]  

The on/off ratio will vary from limit in Eq. (4) to Eq. (5) for intermediate values of \( L \). For simplicity we assume that \( R_M, R_S \) and \( \rho_M \) are independent of \( V_g \) while \( \rho_S \) depends on \( V_g \) (this assumption needs further justifications) i.e. the on/off ratio \( S(L \to 0) \) is independent of \( V_g \) while \( S(L \to \infty) \) depends on \( V_g \) at which the on current is defined. The observation that the on/off ratio increases with \( L \) implies that \( R_M/R_S < \rho_M/\rho_S \) for given \( V_g \). Figure S4 shows measured (symbols) and curve fit (lines, using Eq. 3) on/off ratio vs. \( L \) for different values of \( V_g \). Specifically, if \( V_g \) is reduced, the s-SWNTs have lesser current (\( \rho_S \) higher) and slope of the curve decreases as expected. With this set of data, it is possible to extract parameters by curve fitting, but the accuracy of such a process in this case is limited to do the small number of data points.

**Resistance of metallic SWNTs**

Figure S5 shows the \( I_D-V_D \) plot for primarily the metallic tube contribution to the current (here \( V_G = 10 \) V so the semiconducting tubes are mostly off). The metallic tubes show lower resistivity at low bias and higher resistivity at high bias, which can be observed in most clearly for the case of the 5 \( \mu \)m channel length case.

At low bias, only acoustic phonons which have a higher mean free path (\( \lambda \sim 1.5 \) \( \mu \)m) (Ref. 1, 2) are present in metallic tubes. On the other hand at high bias, the optical phonons dominate (\( \lambda \sim 15-20 \) nm) and the resistivity increases. The transition point comes roughly when the electric field is high enough to have a voltage drop of \( \sim 160 \) mV (which is optical phonon energy) in one mean free path.

Figure S5 also shows in the plot of \( I_D \) vs. \( V_D/L \) all 4 curves lay roughly on top
of each other with the saturation point roughly at $V_D/L \sim 0.5 \text{ V } \mu\text{m}^{-1}$.

Figure S6 shows a scaling plot of the low bias resistances as a function of channel length. The zero intercept indicates small overall influence of contacts in these devices. The high and low bias resistivity values for various references including the present work are also presented.

From the scaling plot, the slope = $300 \Omega \mu\text{m}^{-1}$. Each of the transistors have roughly 1000 SWNTs and 1/3 of them for m-SWNTs and approximately >80% of all the tubes bridge S/D.

The resistivity can be estimated as

$$300 \times 1000 \times 1/3 \times 0.8 = 80 \text{ k}\Omega \mu\text{m}^{-1}.$$ 

This value is significantly higher than the best observed values for single tubes ~6 kΩ μm$^{-1}$. The high bias resistance is somewhat lower than observations in single tubes.


**Devices with different tube densities**

We fabricated a series of devices with different tube densities, $D$. Figure S7 presents transfer curves for representative devices. Qualitatively, the responses are similar to those of the high density devices presented in the main text and in Fig. 1.

**Gate capacitance and mobility**

Mobility calculation requires knowledge of the charge density of a single SWNT in the channel and the average drift electric field: $\mu = I / (\rho E)$. We estimate the latter as $V_d/L$. The former depends on the gate voltage according to $\rho = C_t V_g$, where $C_t$ is the specific capacitance per unit length of the single tube in the array, which depends on the device geometry. We define the field-effect mobility as

$$\mu = \frac{L}{V_d C_t} \frac{dI}{dV_g}.$$
for the single SNWT current channel and similarly for the effective field-effect mobility of the TFT device as

\[ \mu = \frac{L}{V_g C_W W} \frac{dI}{dV_g} \]

where \( C_W \) is the specific capacitance per unit area. For example \( C_W = \varepsilon_o \varepsilon_{ins} / d \) is the specific capacitance (per unit area) of the plate capacitor. This definition of mobility is valid even in the presence of metallic nanotubes since the current through these tubes is independent of \( V_g \). The current can be written as \( I = I_M + I_S(V_g) \) and hence \( dI/dV_g = dI_S(V_g)/dV_g \).

The relation between \( C_W \) and \( C_t \) is important for our conclusions on the TFT performance. In order to obtain the total charge density (and current) of the TFT device with \( D \) tubes per unit width we have to multiply the single tube capacitance by \( D \):

\[ C_W = D \cdot C_t \]

As we have shown in Ref.[S. V. Rotkin, in *Applied Physics of Nanotubes*, (Ed: Avouris P.), Springer Verlag GmbH Co., KG 2005.] the SWNT capacitance has two contributions: the quantum one and the geometrical one. The former is given by the SWNT density of states: \( C_Q = e^2 g_o \sim 3.2 \) [S. Rosenblatt, Y. Yaish, J. Park, J. Gore, V. Sazonova, P. L. McEuen, *Nano Lett.* 2002, 2, 869. K. A. Bulashevich, S. V. Rotkin, *Jetp Lett.* 2002, 75, 205.]. The latter has been recently derived by us for an infinite array of parallel SWNTs with uniform spacing \( 1 / D \) in:

\[ C^{-1}_{array} = \frac{1}{2\pi \varepsilon_0 \varepsilon_s} \cdot \log \left[ \frac{\sinh(2\pi D)}{\pi RD} \right] \]

where \( R \) is the SWNT radius, \( t \) is the distance to the gate electrode, \( \varepsilon_s \) is the dielectric constant of the surface/interface where we place the tubes. For the SWNT in the quartz/SWNT/SU-8 sandwich structure the dielectric constant \( \varepsilon_s = (\varepsilon_{SiO_2} + \varepsilon_{SU-8}) / 2 \approx 4 \) due to the low dielectric contrast between these materials: quartz substrate (\( \varepsilon_{SiO_2} = 4.1 \)), gate dielectric (SU-8 Epoxy, \( \varepsilon_{SU-8} = 3.9 \)), corresponding distribution of the electrostatic potential is shown in Fig. S8f. For the case of the SWNT array been transfer at the quartz or resin surface, the effective capacitance is half of the substrate capacitance \( \varepsilon_s = (\varepsilon_{SiO_2}/2 + 1) / 2 \approx 2 \) where 1 is the dielectric permittivity of the air (see Fig. S8d).
The specific capacitance per unit area for the SWNT TFT has an analytical expression:

\[
C_w = D \cdot C_t = \left[ \frac{D}{C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_s} \cdot \log \left( \frac{\sinh(2\pi D)}{\pi RD} \right)} \right]
\]

This expression allows series expansion in a small unit-less parameter \(1 / (D t)\) which is just the number of SWNTs in an area of the width \(t\), where the tubes are still electrostatically coupled. The tubes at the longer distances are completely screened by the gate, as shown in Fig. S8a-c. Then the specific capacitance reads as:

\[
C_w = \frac{D \varepsilon_0 \varepsilon_s}{\varepsilon_0 \varepsilon_s C_Q^{-1} + \frac{1}{2\pi} \cdot \log \left( \frac{\exp(2\pi D)}{2\pi RD} \right)} = \frac{D \varepsilon_0 \varepsilon_s}{\varepsilon_0 \varepsilon_s C_Q^{-1} + \left( tD - \frac{1}{2\pi} \log(2\pi RD) \right)}
\]

\[\approx \frac{\varepsilon_0 \varepsilon_s}{t} \cdot \left[ 1 + o(1/(Dt)) \right]\]

where in last expression we single out terms of the order of \(1/(Dt)\) and smaller that must be neglected for the dense array \(D >> 1 / t\).

This expression allows us to estimate the TFT drain current as

\[
I_d = WD_{SWNT} = WDC_t V_g \frac{V_d}{L} = WV_g V_d \frac{\varepsilon_\infty \varepsilon_s}{t} \cdot \left[ 1 + o(1/(Dt)) \right]
\]

We can draw two conclusions: (1) this formula shows that the capacitance coupling of the SWNT TFT with the density higher than the inverse distance to the gate \(D > 1 / t\) is almost equal to the capacitance of the solid metal plate channel of the same geometry. (2) the effective mobility of the SWNT TFT saturates at this density due to the inter-tube screening: even though we may increase the number of current channels per unit width by increasing \(D\), the overall current will be approximately constant due to lower charge density per individual channel. We note that this analysis does not consider fringing field effects due to the finite length of the TFT device which effects would result in slightly underestimated capacitance.

Figure S9 shows the capacitance of the array for different tube densities. The derivation assumes that the tube-tube distance and tube diameters are constant. Numerical values of the gate capacitance can be calculated by finite element technique. Scatter plot shows the values calculated in this way. The FEM results and the
analytical expression show very good agreement for all densities. For very low density case where \( D << 2t \) analytical expression goes to single tube values. Our tube densities are typically between 1 SWNT \( \mu m^{-1} \) to 8 SWNT \( \mu m^{-1} \). We have built devices with different gate dielectric thickness (from 10 nm to 1.5 \( \mu m \)). If the gate thickness is much larger than the tube-tube distance, the array can be assumed as continuous film and the parallel plate capacitance can be used.

The capacitance of the SWNT array has a weak (log) dependence on the inter-tube distance \( 1/D \). We have shown that the result for the capacitance coupling is only weakly sensitive to deviations from the even spacing assumption used in the above analysis. Numerical simulation confirms that variations in \( D \) in different parts of a single device do not contribute any significant correction to the capacitance value (Fig. S8g).

In the regime of \( D >> 1/t \) we may also neglect the variation in the number of tubes per device. Even though the smaller number of tubes per device width means a bit smaller number of current channels it means also better capacitance coupling according to our formula above. These two effects tend to cancel each other.

**Electrical breakdown process**

One method to obtain high on/off ratios involves electrical breakdown of the metallic nanotubes. For the devices described here, this process involved sweeping the drain voltage from 0 V to negative values while holding the gate voltage at +20 V. Multiple sweeps, up to voltages of 50 V, eventually eliminated virtually all of the off state current in the devices. The current reductions tended to occur in well-defined steps of ~25 \( \mu A \), consistent with expectation based on single tube device studies. Figure S10 summarizes some aspects of these procedures, as performed on devices that consist of \( D = 4 \) SWNT \( \mu m^{-1} \), \( L = 12 \mu m \), \( W = 200 \mu m \) on SU8 (150nm)/SiO\(_2\) (100nm)/Si substrate with 100 nm Au layer source and drain electrodes.

**Transfer of the SWNT arrays**

The transfer procedures outlined in the main text provide reproducible and high yield operation. Figure S11 shows SEM images of representative SWNT arrays on their growth substrate and after transfer onto a target substrate. These images show no loss of alignment, degree of linearity after transfer. In addition, to within uncertainties associated with the imaging, >99% of the SWNTs are transferred using this procedure. Figure S12 shows a bare growth substrate after transfer, indicating the high yields associated with removal of the tubes.
Device Yields

The overall yields of the high performance devices of Fig. 4 result from the combined yields of the growth procedures and the lithographic and deposition processes used to define the electrodes and dielectric layers. The results of Fig. 4 illustrate the typical scatter in the device properties. The yields are >80%, with defects that are typically associated with the liftoff and etching procedures used to define the source, drain and gate electrodes. Figure S13 presents optical images that show two examples of this class of defect.

High frequency response

High-frequency characteristics were measured in the common-source configuration using an Agilent E5062A network analyzer and Cascade Microtech RF-1 probe station. Figure S14 shows the current gain ($H_{21}$) versus frequency ($f_T$) for a drain bias ($V_D$) of 2 V and a gate bias ($V_G$) of 0 V. The $f_T$ value was 420 MHz for a device with $L = 4 \mu$m and $W = 300 \mu$m.
Supplementary Figures

**Supplementary Figure S1:**  
a, SEM image of an array of SWNTs showing 99.97% alignment. The inset shows the single, small segment of a misaligned tube that exists in this entire area.  
b, AFM image of an array of SWNTs showing excellent parallelism.
c, Plot of deviation in the position of a SWNT as a function of position along its length, measured relative to a perfect linear shape. To within the uncertainties of the AFM instrument, the SWNT is perfectly linear.  

d, Distribution of SWNT diameters measured from an array like that shown in a.  
e, Diameters of SWNT measured as a function of position across an array.  
f, Distribution of SWNT lengths in an array similar to that shown in Fig. 1a of the main text.  
g, Measured numbers of SWNTs that bridge the gap between source and drain electrodes spaced by some distance (i.e. the channel length).  
h, Distribution of radial breathing mode frequencies as measured by Raman scattering from individual tubes in an array.  
i, Measured on currents in transistors (TFTs) with different channel lengths ($L$).
Supplementary Figure S2: Growth yield for nanotube arrays. Five substrates with patterned Fe catalyst were prepared and tubes were grown on them by CVD.
Supplementary Figure S3:  Scanning electron micrograph (a) and transfer curves (b) from devices built with single tubes.
Supplementary Figure S4: Experimental (symbols) and curve fitting (lines, using Eq. 3) for on/off ratio vs. L for different values of $V_g$. 
Supplementary Figure S5: Current/voltage characteristics of metallic tube contributions to device response, as a function of channel length for the case of D = 5 SWNT μm⁻¹.
Supplementary Figure S6: Scaling plot (top frame) of resistance, evaluated in the low bias regime, associated with metallic contribution to device response as a function of channel length, for the case of $D = 5$ SWNT $\mu$m$^{-1}$. Low and high bias resistances (bottom frame) evaluated in the present paper to two other references.
Supplementary Figure S7:  a-d, Transfer curves measured from typical devices with $V_D = -0.5$ V ($D = \sim 5, 1, 0.6, 0.3$ tubes $\mu$m$^{-1}$), which were used for figure 2e. The channel length and width were 10 $\mu$m and 200 $\mu$m, respectively, and 1.5 $\mu$m epoxy layer was used as a gate dielectric.
**Supplementary Figure S8:**  

- **a-c,** Electrostatic potential distribution for the NT-array TFT embedded in the insulator with dielectric constant $\varepsilon = 3.9$, the NT radius is 0.7 nm, the insulator thickness is 1500 nm, the tube densities are 0.2, 0.4 and 2 tubes $\mu m^{-1}$ for **a**, **b** and **c** respectively. The spots corresponding to nanotubes are artificially large because it may not be seen at this size scale.  

- **d-f,** Electrostatic potential distribution for the NT-array TFT embedded in between two layers of the insulator with the dielectric constants (**d** $\varepsilon = 4.1 / 1$, **e** $\varepsilon = 3.9 / 3.9$ (same as in **a** above), **f** $\varepsilon = 3.9 / 4.1$), the NT radius is 0.7 nm, the insulator thickness is 1500 nm, the tube density is 0.2 tubes $\mu m^{-1}$.  

- **g,** The range of a random variation of the TFT array capacitance after 1/3 of tubes (metallic
tubes) are destroyed. h, Three sample (random) distributions of the tubes left after destruction of metallic tubes. As shown in g the capacitance decreased by 14-36% for the NT-array TFT embedded in the insulator with dielectric constant $\varepsilon = 3.9$, the NT radius is 0.7 nm, the insulator thickness is 250 nm, the tube density is 4 tubes/micron. In this figure the bar scale is 1 $\mu$m.
Supplementary Figure S9: Modeling results for the capacitance between an array of conducting wires and a gate electrode, separated by a dielectric as a function of dielectric thickness.
Supplementary Figure S10:  
a, Current-voltage response of a device during electrical breakdown procedures.  
b, Schematic illustration of a device.  
c, Calculated field effect mobility as a function of on/off ratio.  
d, On and off currents as a function of on/off ratio.
Supplementary Figure S11: Transfer yields for nanotube arrays. The SEM images on the left show the nanotube arrays on quartz before transfer. The images on the right show the nanotube arrays on 10 nm HfO$_2$. 
Supplementary Figure S12: SEM image of a quartz substrate after transfer nanotube arrays. There are no remaining tubes on the substrate.
Supplementary Figure S13: Optical images that indicate the sorts of imperfections that are associated with defective devices.
Supplementary Figure S14: Measurement of the small signal current gain (H21) as a function of frequency. The results indicate a cutoff frequency value of $f_T = 420$ MHz.